REMARKS

Claims 1-2, 6, 12-16, 21-32 are pending and are rejected. Claims 23 and 28 are cancelled, however Applicants reserve the right to pursue these claims in a divisional or continuation application. Reconsideration and allowance of Claims 1-2, 6, 12-16, 21-22, 24-27, and 29-32 are respectfully requested.

Rejection of Claims under 35 USC §102

Claims 1-2, 6, 12-16, 21-22, 24-27, and 29-32 are rejected under 35 USC §102(b) as being anticipated by U.S. Patent No. 4,947,366 to Johnson. Applicants respectively traverse these rejections.

Johnson discloses a data transfer controller (DTC) that transfers data between a first bus having high performance devices such as a CPU coupled thereto and a second bus having low performance devices such as peripherals coupled thereto in a manner that does not degrade operation of the high performance devices. Further, because Johnson's DTC includes a set of I/O ports and a separate set of direct memory access (DMA) channels, Johnson's DTC may advantageously interconnect multiple buses having different performance characteristics and may also advantageously allow I/O port and DMA operations to be overlapped (See Johnson, col. 1 lines 15-23 and lines 51-65, and col. 2, lines 1-22).

During DMA transfers, Johnson's DTC includes a Local Byte Count Register that indicates the number of bytes successfully transferred. When this count matches or exceeds the value in the Terminate Count Register, the DMA channel transfers are complete and may be terminated. Thus, DMA transfers in Johnson's DTC are terminated when the terminate count is reached, as determined by the DTC (see Johnson, col. 16, lines 46-64, col. 30, lines 48-55, and col. 31, lines 1-8). Johnson is silent about an I/O device generating an early termination request signal that results in termination of the DMA transfer.

Claim 1 of the present application recites:

> A system comprising:
> a direct memory access (DMA) controller; and
> an input/output (I/O) device coupled to the DMA controller, wherein the DMA controller terminates a DMA transfer and clears a current transfer counter before a terminal count is reached upon receiving an early termination request

signal from the I/O device.

Applicants respectively submit that Johnson fails to disclose or suggest receiving an early termination request signal from an I/O device during a DMA transfer. Further, Johnson fails to disclose or suggest a DMA controller that terminates a DMA transfer upon receiving an early termination request signal from an I/O device before a terminal count is reached.

To anticipate a claim under 35 USC §102, each and every element of the claim must be disclosed in a single reference[1]. The exclusion of a claimed element, no matter how insubstantial or obvious, from a prior art reference is enough to negate anticipation under 35 USC §102.[2] Thus, because Johnson fails to disclose or suggest "an input/output (I/O) device coupled to the DMA controller, wherein the DMA controller terminates a DMA transfer and clears a current transfer counter before a terminal count is reached upon receiving an early termination request signal from the I/O device," as recited in Applicants' Claim 1, Claim 1 is not anticipated by Johnson.

The Examiner asserts that Johnson discloses at col. 29, lines 1-65 "the termination of a DMA transfer before a terminal count is reached" (See Office Action, page 3, paragraph 5). Applicants disagree.

First, as indicated above, Johnson's DTC includes separate I/O ports and DMA channels. The language referred to by the Examiner describes various exception conditions for transfers handled by Johnson's I/O ports, not for DMA transfers handled by Johnson's DMA channels (see Johnson, col. 29, lines 1-3), and therefore does not anticipate Applicants' Claim 1. Second, the Examiner has not pointed to any language in Johnson that discloses or suggests receiving an early termination request signal from the I/O device during a DMA transfer, as recited in Applicants' Claim 1. Accordingly, Applicants respectfully request the Examiner to withdraw the rejection of Claim 1.

Claims 2, 6, and 24-27 depend from Claim 1 and therefore distinguish over the cited references for at least the same reasons as Claim 1.

Claim 12 recites:

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1 Corning Glass Works v. Sumitomo Electric, 9 USPQ2d 1962, 1965 (Fed. Cir. 1989).
2 Connell v. Sears, Roebuck & Co., 220 USPQ 193, 198 (Fed. Cir. 1983).

A system comprising:
a direct memory access (DMA) controller; and
an input/output (I/O) device coupled to the DMA controller, wherein the DMA controller re-executes a DMA transfer from the beginning with the I/O device upon receiving a retransmit request signal from the I/O device.

Applicants respectively submit that Johnson fails to disclose or suggest receiving a retransmit request signal from an I/O device. Further, Johnson neither discloses nor suggests a DMA controller that re-executes a DMA transfer upon receiving a retransmit request signal from the I/O device, as recited in Applicants' Claim 12, and therefore Claim 12 is not anticipated by Johnson.

The Examiner refers to col. 29, lines 32-42 of Johnson as support for his assertion that Johnson teaches "the re-executing of a DMA transfer from the beginning upon the receiving of a request signal," and then concludes that "it is inherent that the signals required to restart the access and subsequent transfer are used with this system in order to execute the transfer. Applicants disagree.

The language referred to by the Examiner describes a restart operation for transfers handled by Johnson's I/O ports, not for DMA transfers handled by Johnson's DMA channels (see Johnson, col. 29, lines 1-3), and therefore does not anticipate Applicants' Claim 12. Further, the Examiner has not pointed to any language in Johnson that discloses or suggests receiving a retransmit request signal from the I/O device during a DMA transfer, as recited in Applicants' Claim 12.

In addition Applicants request a reference for the Examiner's assertion that in claim 12 for the feature "the DMA controller re-executes a DMA transfer from the beginning with the I/O device upon receiving a retransmit request signal from the I/O device", that it is inherent in Johnson that the a transmit request signal come from the I/O device. Otherwise, the Applicants assert the Examiner's assertion is merely conclusory and based on hindsight and should be withdrawn.

Accordingly, because Johnson fails to disclose or suggest "an input/output (I/O) device coupled to the DMA controller, wherein the DMA controller re-executes a DMA transfer from the beginning with the I/O device upon receiving a retransmit request signal from the I/O device," as recited in Applicants' Claim 12, Claim 12 is patentable over Johnson.

Claims 29-32 depend from Claim 12 and therefore distinguish over the cited references for at least the same reasons as Claim 12.

Claim 13 recites:

> A method comprising:
> transferring data between a first device and a second device under control of a direct memory access (DMA) controller;
> receiving a request signal at the DMA controller from the first device indicating a request by the first device to re-transmit the data between the first device and the second device;
> transmitting an acknowledge signal from the DMA controller to the first device; and
> re-transferring the data from the beginning between the first device and the second device.

For the reasons described above with respect to Claim 12, Claim 13 is also patentable over Johnson. Specifically, Johnson fails to disclose or suggest "receiving a request signal at the DMA controller from the first device indicating a request by the first device to re-transmit the data between the first device and the second device," as recited in Claim 13, and therefore Claim 13 is not anticipated by Johnson.

The Examiner refers to col. 29, lines 32-42 of Johnson as support for his assertion that Johnson teaches "the re-executing of a DMA transfer from the beginning upon the receiving of a request signal." However, as discussed above with respect to Claims 1 and 12, the language referred to by the Examiner describes various operations for transfers handled by Johnson's I/O ports, not for DMA transfers handled by Johnson's DMA channels (see Johnson, col. 29, lines 1-3), and therefore does not anticipate Applicants' Claim 13. Further, the Examiner has not pointed to any language in Johnson that discloses or suggests receiving a request signal from the I/O device to re-transmit the data, as recited in Claim 13. Accordingly, Claim 13 is patentable over Johnson.

Claims 14 and 16 depend from Claim 13 and therefore distinguish over the cited references for at least the same reasons as Claim 13.

Claim 15 recites:

> A method comprising:
> transferring data between a first device and a second device under control of a direct memory access (DMA) controller;

receiving a request signal at the DMA controller from the first device indicating a request by the first device to terminate the transfer of data between the first device and the second device;

erasing appropriate DMA controller information in order to restart the transfer of data between the first device and the second device;

transmitting an acknowledge signal from the DMA controller to the first device; and

terminating the transfer of data between the first device and the second device.

For the reasons described above with respect to Claim 1, Claim 15 is also patentable over Johnson. Specifically, Johnson fails to disclose or suggest "receiving a request signal at the DMA controller from the first device indicating a request by the first device to terminate the transfer of data between the first device and the second device," as recited in Claim 15, and therefore Claim 15 is not anticipated by Johnson.

The Examiner refers to col. 29, lines 32-42 of Johnson as support for his assertion that Johnson teaches "the termination of a DMA transfer" and "the erasing by reloading the configuration registers with control information." However, as discussed above with respect to Claims 1 and 12, the language referred to by the Examiner describes various operations for transfers handled by Johnson's I/O ports, not for DMA transfers handled by Johnson's DMA channels (see Johnson, col. 29, lines 1-3), and therefore does not anticipate Applicants' Claim 15. Further, the Examiner has not pointed to any language in Johnson that discloses or suggests receiving a terminate request signal from the I/O device during a DMA transfer, as recited in Claim 15. Accordingly, Claim 15 is patentable over Johnson.

Claims 21-23 depend from Claim 15 and therefore distinguish over the cited references for at least the same reasons as Claim 15.

CONCLUSION

In light of the above remarks, it is believed that Claims 1-2, 6, 12-16, and 21-22, 24-27, and 29-32 are in condition for allowance and, therefore, a Notice of Allowance of Claims 1-2, 6, 12-16, and 21-22, 24-27, and 29-32 is respectfully requested. If the

Examiner's next action is other than allowance as requested, the Examiner is requested to call the undersigned at (408) 879-6149.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Commissioner for Patents, P.O. BOX 1450, Alexandria, VA 22313-1450, on March 22, 2005.

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